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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,492	12/01/2003	Chih-Ta Star Sung		1041

7590 02/24/2005

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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,492	SUNG, CHIH-TA STAR	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *9-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated December 01, 2003, claims 1-14 are active in this application.

Claim Objections

2. Claims 9-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-7 are rejected under 35 U.S.C 102(b) as being anticipated by

Kumagai et al. [U.S. Patent #6,255,862].

With respect to claim 1, Kumagai et al. discloses a semiconductor memory sensing circuit in a memory array, comprising: at least one memory cell of a memory array, that generates a first voltage output and a second voltage output when the memory cell is accessed, wherein the first voltage output ramps from a predetermined voltage level to a higher voltage level [column 7], and the second voltage output keeps in a predetermined voltage level [column 7 – indicates that one bit line is higher than the other]; a first N-type device coupled between ground and one corresponding bit line of the memory array [see figure 2]; a second N-type device coupled between ground and one corresponding bit line-bar of the memory array [see figure 2]; and a different amplifier with two input nodes coupled to the bit line and the bit line-bar of the memory array to generate a first sense output voltage if the first voltage output of one memory cell is higher than a second voltage output of the one memory cell and to generate a second sense output voltage if the first voltage output of one memory cell is lower than a second voltage output of the one memory cell [see column 7 – indicates that whether the outputs are high or low, the amplifier amplifies the outputs.

With respect to claim 2, Park further discloses that the memory cell has at least one semiconductor device – sram. See figure 2.

With respect to claim 3, Park further discloses that the memory cell has a static random access memory [sram] device. See figure 2.

With respect to claim 4, Park further discloses that the SRAM cell has at least one back-to-back inverting circuit [MP1, MN1, MP2, MN2 if figure 2] with both inverting

devices hooked up to VDD through a pull-up device and to ground through a pull-down device – see figure 2.

With respect to claim 5, wherein the pull-up device has a P-type semiconductor device [MP1 and MP2] and the pull-down device has a N-type semiconductor device [MN1 and MN2].

With respect to claim 6, the pull-up device has a resistor [parasitic resistance] and the pull-down device has another resistor [parasitic resistance].

With respect to claim 7, wherein the differential amplifier has an amplifier circuit with at least two differential input nodes [N01 and N02 of figure 2] and a control input [SAE of figure 2] for enabling and disabling the amplifier circuit.

5. Claim 8 is rejected under 35 U.S.C 102(b) as being anticipated by Park [U.S. Patent #5,905,688].

With respect to claim 8, Park discloses a control circuit for a semiconductor memory array, comprising: a sense amplifier for amplifying output from a memory cell; and a self-timer coupled to the sense amplifier for counting a time and sending out control signals to shut off the sense amplifier according to the time and pulling down a word line to avoid further current sinking through the memory cell. See column 7, lines 1-25. In the cited section, Park indicates that there exists a power down circuit timer 40 which controls both the sense amplifier and word line. Park further indicates that when word line is disabled in order to inhibit current from flowing from the memory cell.

Allowable Subject Matter

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- A delay device for controlling a second time to discharge a bit line and a bit line bar of the memory array.
- Wherein the self-timer counts the time of differentiating a voltage between the bit line and the bit line bar.
- Wherein when the differential voltage of the bit line and the bit line bar reaches a predetermined threshold, the self-timer sends a signal to turn off the word line.
- Wherein when the differential voltage of the bit line and the bit line bar reaches a predetermined threshold, the self-timer sends a signal to enable the sense amplifier.

Conclusion

7. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit ~~2823~~ 2827
February 18, 2005

MICHAEL TRAN
PRIMARY EXAMINER